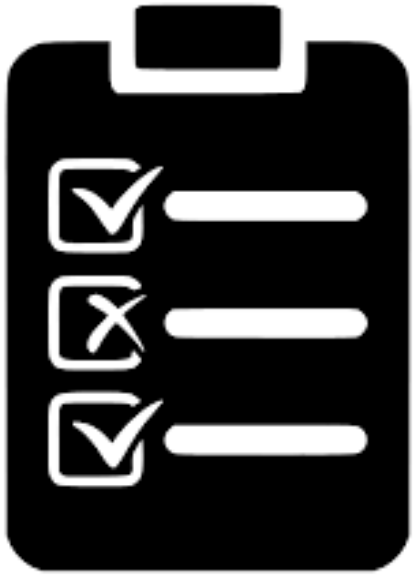
Guidelines for Digital Posters at the SKULL BASECON 2023

Dear Presenters,

We are excited to welcome you to the SKULLBASECON-2023 and appreciate your contribution to the event through your Digital Poster Presentation.

To ensure a cohesive and informative experience for all attendees, please adhere to the following guidelines when creating and presenting your digital posters.

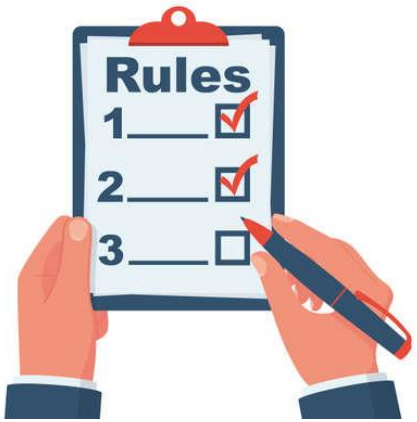


1. Poster Format

- Digital posters should be in landscape orientation.
- The recommended aspect ratio is 16:9 for optimal display on screens.
- Use a high-resolution format to ensure clarity and readability. Format: 1920 x 1080 (Full HD)
- Hyperlinks, animated images and slide transitions, video, music, JPEG will not be accepted.

2. Content Guidelines

- E-poster should not be too cluttered. It should be set out in a clear and logical manner, with reading matter reduced to an essential minimum.
- Lettering, including figure legends, labelling, symbols & graphs etc. should be large enough to be legible when viewed on 48" screen.
- Drawings, diagrams and photos are extremely helpful and often necessary to display results and conclusions.
- Make sure that your illustrations are easy to understand do not overload any chart or drawing with information.



3. Design and Layout

- Maintain a clean and organized layout to enhance readability.
- Please use dark text colors on light backgrounds and readable fonts like **Calibri, Arial and Verdana.**
- **Title**: Size 80 pts or 100 pts, if the title is long, please adjust the size accordingly.
- **Authors**: Size 40 pts to 50 pts, if there are many, its good to use a font with lower size.
- **Main text**: 40-50 pt. although 32 pt. or even 28 pt. is recommended in isolated areas, or if you have a very large amount of text.

4. Visual Elements

- Include high-quality visuals that complement your content.
- Ensure all images and graphs are appropriately labeled and cited.
- Use color sparingly and purposefully; avoid overly bright or clashing color schemes.
- Aim for a balanced mix of text and visuals to engage viewers.

5. File Format

- Submit your digital poster as a Power Point Document.
- Name your file clearly with your name and poster title (e.g., "JohnSmith_SkullBasePoster.pptx").

6. Size and Resolution

- Maintain a reasonable file size for easy sharing and viewing.
- Maximum acceptable size of the file is 10MB.
- Use a resolution of at least 300 DPI to ensure clarity when zoomed in.

7. Interactivity

- Consider adding interactive elements like hyperlinks or QR codes to provide access to additional information or resources.
- Prepare a brief summary or audio narration if applicable.

8. Accessibility

- Ensure your poster is accessible to individuals with disabilities.
- Use alt text for images and provide accessible PDFs if possible.

9. Presentation

- Be prepared to present your digital poster during the assigned session.
- Engage with attendees, answer questions, and provide insights into your research.

10. Technical Requirements

- Test your digital poster on the conference platform or equipment provided in advance to ensure compatibility.

11. Submission Deadline

- Submit your digital poster by the specified deadline to allow for technical review and setup.

Examples of E-Poster

A Full-Adder-Based Methodology for the Design of Scaling Operation in Residue Number System

M. Dasygenis, Member, IEEE, K. Mitroglou, D. Soudris, Member, IEEE, and A. Thanailakis

ABSTRACT (ARIAL 40)

Over the last three decades, there has been considerable interest in the implementation of digital computer elements using hardware based on the residue number system, (RNS) due to the carry free addition and other beneficial characteristics of this system. Scaling operation is one of the essential operations in this number system, and is required for almost every digital signal processing application. Up to now, researchers have suggested costly and low throughput read-only memoy-based approaches to address this need. We also address this need by presenting a novel graph-based methodology for designing high-throughput and low-cost VLSI

BACKGROUND (ARIAL 45)

Over the last three decades, there has been considerable interest in the implementation of digital computer elements using hardware based on the residue number system, (RNS) due to the carry free addition and other beneficial characteristics of this system. Scaling operation is one of the essential operations in this number system, and is required for almost every digital signal processing application. Up to now, researchers have suggested costly and low throughput read-only memoy-based approaches to address this need. We also address this need by presenting a novel graph-based methodology for designing high-throughput and low-cost VLSI RNS scaling architectures, based completely on full adders

OBJECTIVES (ARIAL 32)

Over the last three decades, there has been considerable interest in the implementation of digital computer elements using hardware based on the residue number system, (RNS) due to the carry free addition and other beneficial characteristics of this system. Scaling operation is one of the essential operations in this number system, and is required for almost every digital signal processing application. Up to now, researchers have suggested costly and low throughput read-only memoy-based approaches to address this need. We also address this need by presenting a novel graph-based methodology for designing high-throughput and low-cost VLSI RNS scaling architectures, based completely on full adders

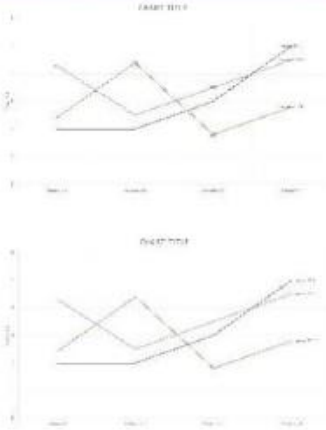
METHODS (ARIAL 50)

Over the last three decades, there has been considerable interest in the implementation of digital computer elements using hardware based on the residue number system, (RNS) due to the carry free addition and other beneficial characteristics of this system. Scaling operation is one of the essential operations in this number system, and is required for almost every digital signal processing application. Up to now, researchers have suggested costly and low throughput read-only memoy-based approaches to address this need. We also address this need by presenting a novel graph-based methodology for designing high-throughput and low-cost VLSI RNS scaling architectures, based completely on full adders

RESULTS (ARIAL 36)

Over the last three decades, there has been considerable interest in the implementation of digital computer elements using hardware based on the residue number system, (RNS) due to the carry free addition and other beneficial characteristics of this system. Scaling operation is one of the essential operations in this number system, and is required for almost every digital signal processing application. Up to now, researchers have suggested costly and low throughput read-only memoy-based approaches to addressa

RESULTS



CONCLUSIONS

Over the last three decades, there has been considerable interest in the implementation of digital computer elements using hardware based on the residue number system, (RNS) due to the carry free addition and other beneficial characteristics of this system. Scaling operation is one of the essential operations in this number system, and is required for almost every digital signal processing application. Up to now, researchers have suggested costly and low throughput read-only memoy-based approaches to address this need. We also address this need by presenting a novel graph-based methodology for designing high-throughput and low-cost VLSI RNS scaling architectures, based completely on full adders

We look forward to seeing your digital posters at the SKULLBASECON-2023 and encourage you to reach out to the conference organizers for any clarifications or assistance.

Your contribution is vital to the success of the event, and we appreciate your dedication to advancing knowledge in the field of Skull and Brain Research.